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## APPLICANTS

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## \*\* CONTINUING DATA \*\*\*\*\*

NONE JAT

## \*\* FOREIGN APPLICATIONS \*\*\*\*\*

JAPAN 2000-266971 09/04/2000

YES JAT

## IF REQUIRED, FOREIGN FILING LICENSE GRANTED

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Foreign Priority claimed	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	STATE OR COUNTRY JAPAN	SHEETS DRAWING 13	TOTAL CLAIMS 11	INDEPENDENT CLAIMS 1
35 USC 119 (a-d) conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged	<i>[Signature]</i> <input type="checkbox"/> Examiner's Signature <i>JAT</i> Initials				

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## TITLE

Semiconductor integrated circuit with suppressed clock skew

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